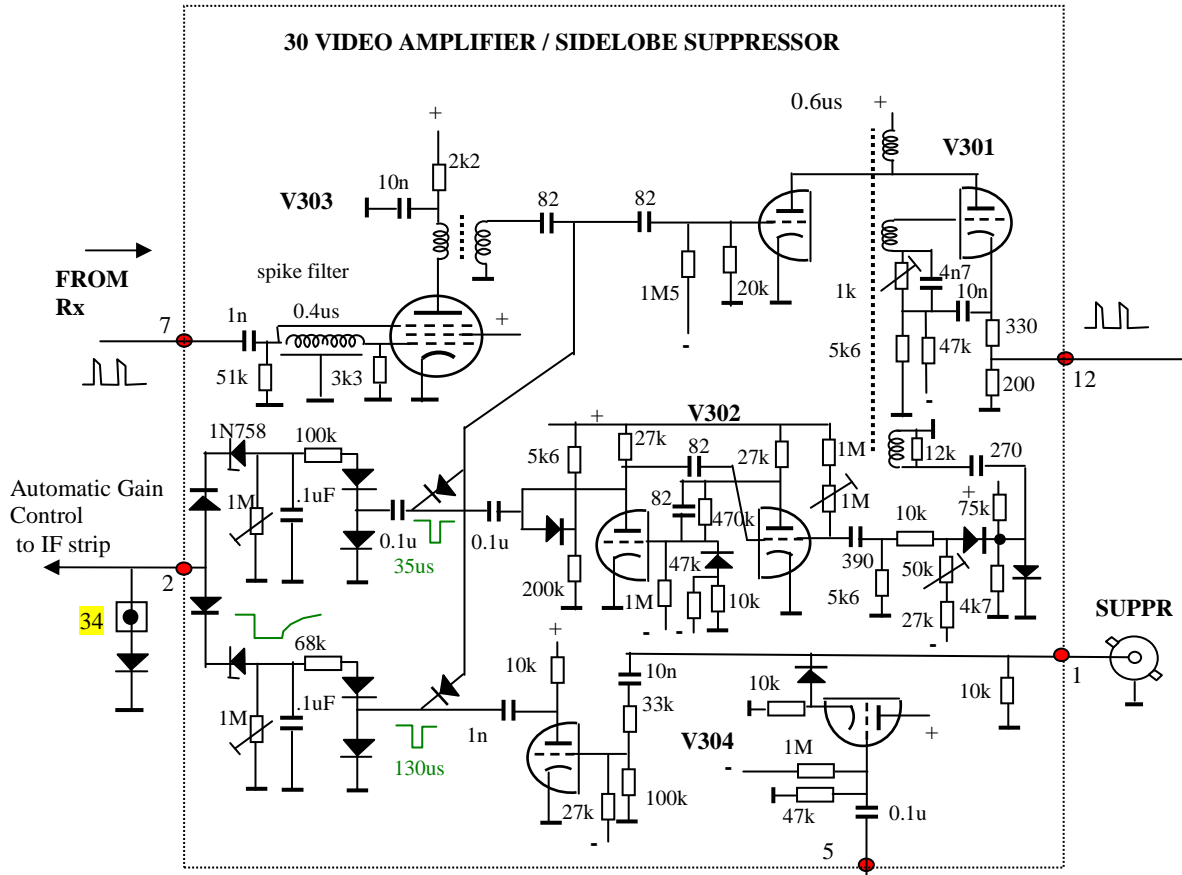


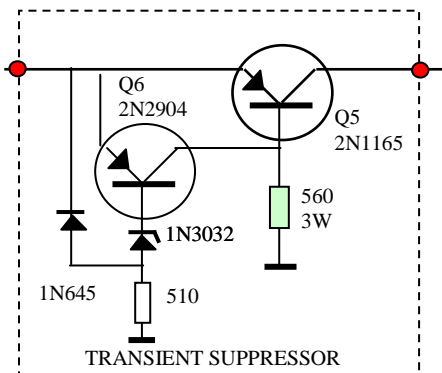
# APX44B Modifications

Around 1968, the APX-44 (introduced in 1960) could be upgraded to the APX-44B adding sidelobe suppression (SLS) from the ground antenna, and transient suppression from the 27Vdc bus. The upgrade contains a new Video Amplifier, and a small transient protection unit in series with the DC input fuse. Both are described here.

1. The video amplifier/SLS card replaces the old video amplifier and is pin-compatible. The ground antennae sends a SLS pulse over an omnidirectional antenna, 2us after the first pulse of each double-pulse pair, at a lower amplitude than each of the double pulses.



A blocking oscillator shapes the received pulses to 0.6us wide pulses with fixed amplitude. The circuitry around V302 detects the new SLS pulse if present, at 2us after the first pulse. If present, a 35us pulse blocks the third pulses, as well as the IF amplifier.



## 2. Transient protector

This circuit is placed in series with the 27.5V input fuse. If the input voltage has a surge above 33V, then the first transistor starts to conduct, shorting emitter and base of the main transistor, which will block the surge.

## Sidelobe-suppression

The three-pulse, sidelobe-suppression type interrogation system uses an added pulse, designated P2, for transponder control. A radar ground station transmits this pulse at a fixed separation ( $2\mu\text{s}$ ) from the first interrogation pulse but at an amplitude considerably **lower** than that of the interrogation first (P1) and last pulse (P3). Sidelobe control pulse P2 is transmitted omnidirectionally around the ground station with an amplitude that exceeds that of any sidelobe being radiated by the radar antenna and is able to initiate transponder set control before the radar antenna side lobes can cause erratic replies.

Spike suppressor V303 eliminates pulses of  $0.3\ \mu\text{sec}$  or less in width and decreases the width of each interrogation pulse by  $0.3\ \mu\text{sec}$  to eliminate most of the received noise pulses. Sidelobe blocking oscillator V301 receives interrogation pulses from V303 and is adjusted to produce output pulses that are approximately  $0.6\ \mu\text{sec}$  in width while maintaining the original interrogation pulse separation. The reshaped interrogation pulses from V301 are applied to all three decoders (V351, V352 and V353). When one of the decoders receives a correct code and mode, main gate multivibrator V404 is triggered. Passage of the SLS control pulse (P2) to the video amplifier/ SLS card input is possible only when pulse P2 has an amplitude sufficient to overcome IF suppressors CR204 through CR207.

Pulse P2 must have an amplitude that exceeds the 10-dbm threshold of the IF suppressor circuit at the  $2.0\text{-}\mu\text{sec}$  separation point to be fed to spike suppressor V303 for triggering of V301. Decoders V351, V352, and V353 will reject the P2 pulse if there is a lack of pulsepair coincidence. Pulses P1 and P2 from V301 are combined and made additive when properly spaced. This action produces a single pulse of sufficient amplitude to trigger sidelobe multivibrator V302. The  $35\text{-}\mu\text{sec}$  output pulse produced by V302 is used to blank V301, suppressing P3, and to prevent decoding of pulse P3. It is also rectified by **automatic overload control** (AOC) rectifier CR308 to reduce IF amplifier (V202, V203 and V204) sensitivity when the preset prf has been exceeded.

For equipments with SLS, the negative main gate pulse from V404 is amplified by main gate amplifier V454A and is applied to suppressor cathode follower and inverter amplifier. The output of V304 cuts off sidelobe blocking oscillator V301 for the duration of the main gate and prevents interrogation of the transponder during the cutoff period. Amplifier V304 also supplies the main gate suppression pulse to SUPPR jack J106 and to main gate AOC rectifier CR305, where the gate is rectified and is applied as bias to IF amplifiers V202, V203, and V204 when the preset prf rate is exceeded. This governs receiver sensitivity by the interrogation repetition rate, and prevents the excessive transmitter duty cycle that would result if the transponder set replied to all interrogations.

A third winding (5-6) on transformer T301 is damped by resistor R339 to prevent ringing and this winding supplies blocking oscillator pulses through capacitor C303 to the sidelobe detector circuit. Sidelobe-suppression gate pulses from V302 are fed to the trigger input of V301 through diode CR303 to cut off V301 immediately after the receipt of an SLS control pulse (P2). The negative sidelobe-suppression gate pulse cuts off V301 to prevent interrogation pulses P3 from reaching decoders V351, V352, and V353 and thus prevents replies in accordance with control pulse P2. Negative main gate pulses from V304 are fed to the trigger input of V301 through diode CR304 to cut off V301 after one proper interrogation is received. Diodes CR303 and CR304 form an OR gate which permits either gate to cut off the trigger section of blocking oscillator V301.

*d. Sidelobe Detector* (fig. 20.1). Sidelobe detector diode CR302, in conjunction with capacitor C303 and resistor R309, forms a memory circuit for the sidelobe blocking oscillator (V301) pulses triggered by interrogation pulse P1. Diode CR302 is forward biased by voltage divider resistors R308 and R309 and the +125-volt dc bus. During the time that V301 is cutoff (no pulse output), capacitor C303 is discharged to ground due to low resistance of CR302. When V301 is triggered by P1 only, the output negative swing of T301 winding 5-6 cuts off CR302 and the negative pulse portion of the output is developed across R309. As the voltage across winding 5-6 goes through the reference level in the positive direction, CR302 again conducts and effectively grounds one side of capacitor C303.

Capacitor C303 then charges to the positive peak voltage across T301 winding 5-6 developed by the positive pulse portion of V301 output. As the positive pulse begins to go negative toward the reference level, diode CR302 again cuts off and capacitor C303 discharges developing the second negative pulse across R309. The separation time between the first negative pulse and the second negative pulse (P1 memory pulse) is the sum of the blocking oscillator output pulse widths (negative and positive swings), and the RC time constant of C303 and R309 determines aperture (memory pulse width), which results in a P1 memory pulse position of approximately 2.0  $\mu$ sec. Triggering of blocking oscillator V301 by a P2 SLS pulse at 2.0  $\mu$ sec results in an overlap of the blocking oscillator negative output pulse and the P1 memory pulse; the P2 memory pulse is of no importance to circuit operation. The P2 pulse and the P1 memory pulse are additive and result in a single pulse approximately double the amplitude of either of the two pulses developed by P1 alone. Diode CR301 is biased to cutoff by a voltage developed across voltage divider resistors R310, R311, R312, and R313 connected between ground and a -150-volt dc bus. The amount of negative bias is adjusted by control R311 to prevent CR301 from conducting on a P1 pulse only. However, when a P2 pulse is added to the P1 memory pulse, the resultant amplitude is enough to cause CR301 to conduct the P2 pulse to R312 and R313. Capacitor C304 couples the P2 pulse to the input of sidelobe multivibrator V302.

*e. Sidelobe Multivibrator* . Grid pin 2 of tube V302 is biased positive by resistors R314 and R315 connected to the +125- volt dc distribution bus to cause plate current saturation. Identical plate load resistors R317 and R318 are used for both sections of tube V302, and grid pin 7 is negative biased with voltage divider resistors R319 and R320 connected from the -150-volt dc distribution bus to plate pin 1. Capacitors C305 and C306 are feedback coupling capacitors. When a negative sidelobe detector trigger pulse is coupled through capacitor C304 to grid pin 2, pin 1 plate current is driven to cutoff; this action drives grid pin 7 positive. Grid pin 7 going positive, increases pin 8 plate current and the negative plate voltage swing is coupled back through C305 to hold grid pin 2 at cutoff. The sidelobe detector trigger pulse has collapsed by this time, pin 1 plate current is cut off, and pin 8 plate current has reached saturation.

The multivibrator pulse width is determined by the discharge rates of capacitors C305 and C306 and the setting of R315. Adjustment is made for a pulse width of 35  $\mu$ sec and the negative sidelobe gate pulse is taken from plate pin 8. Capacitor C307 is the coupling capacitor for input through OR gate diode CR303 to blank V301 for sidelobe suppression (*d* above). Diode CR314 clips any positive peaks occurring on the gate pulse and aids in decreasing pulse delay time which shortens re-initiation time after sidelobe suppression. Diode CR314 has its cathode biased positive by voltage supplied from the +125-volt dc bus through voltage divider resistors R342 and R343, and limits the positive swing of plate pin 8. Diode CR315 has its anode biased negative by voltage supplied from the -150-volt dc distribution bus through voltage divider resistors R340 and R341, and limits the negative swing of grid pin 7 to decrease re-initiation time after sidelobe suppression. This action steepens the leading and trailing edges of the sidelobe gate pulse obtained from multivibrator V302.